

INSTRUCTION FETCH APPARATUS FOR WIDE ISSUE
PROCESSORS AND METHOD OF OPERATION

ABSTRACT OF THE DISCLOSURE

There is disclosed a data processor containing an instruction
5 issue unit that efficiently transfers instruction bundles from a
cache to an instruction pipeline. The data processor comprises
1) an instruction pipeline comprising N processing stages; and
2) an instruction issue unit for fetching into the instruction
pipeline instructions fetched from the instruction cache, each of
the fetched instructions comprising from one to S syllables. The
instruction issue unit comprises: a) a first buffer comprising S
storage locations for storing up to S syllables associated with the
fetched instructions, each of the S storage locations storing one
of the one to S syllables of each fetched instruction; b) a second
15 buffer comprising S storage locations for storing up to S syllables
associated with the fetched instructions, each of the S storage
locations for storing one of the one to S syllables of each fetched
instruction; and c) a controller for determining if a first one of
the S storage locations in the first buffer is full, wherein the
20 controller, in response to such a determination, stores a
corresponding syllable in an incoming fetched instruction in one of
the S storage locations in the second buffer.